REMARKS

The Office Action of 01/16/2008 has been carefully considered. Reconsideration in view of the present remarks is respectfully requested.

Claim 6 was indicated as containing allowable subject matter, which indication is appreciatively acknowledged.

Claims 1-5 were rejected as being unpatentable over Van der Zee in view of Itou. This rejection is respectfully traversed.

The teachings of Itou are essentially unrelated to those of Van der Zee. Itou teaches the use of a noise shielding structure between a semiconductor substrate and power supply buses. Itou has nothing to do with *compensation* of parasitic capacitance, particularly within a resistive divider circuit. Figure 7b of Itou merely illustrates the manner in which the noise shielding structure prevents noise coupling.

It would not have been obvious to apply the teachings of Itou to the circuit of Van der Zee, since the noise sources present in Itou are not present in Van der Zee. Even if the teachings of Itou were applied to the circuit of Van der Zee, the noise shielding structure would not perform the function of compensating for parasitic capacitance as claimed.

Nor would it have been obvious in view of Itou to modify the circuit of Van der Zee to change the location of the compensating structure of Van der Zee to be located underneath the resistor structure of Van der Zee instead of above the resistor structure of Van der Zee. The fact that Itou has a different structure for a different purpose located within the metal/dielectric stack of an integrated circuit does not by itself suggest any such modification.

Accordingly, claim 1 is believed to patentably define over the cited references.

Claims 1-5 were rejected as being unpatentable over Van der Zee in view of Hopper. This rejection is respectfully traversed.

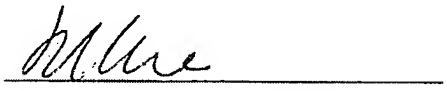
Hopper relates to a technique of minimizing the variation of parasitic capacitance between traces of an integrated circuit by forming an intermediate trace that projects partially in between the traces. Hopper has nothing to do with *compensation* of parasitic capacitance, particularly within a resistive divider circuit. Hopper is in fact unconcerned with the value of parasitic capacitance but is concerned only that variation of parasitic capacitance be kept within a predictable range.

Nor would it have been obvious in view of Hopper to modify the circuit of Van der Zee to change the location of the compensating structure of Van der Zee to be located underneath the resistor structure of Van der Zee instead of above the resistor structure of Van der Zee. The fact that Hopper has a different structure for a different purpose located within the metal/dielectric stack of an integrated circuit does not by itself suggest any such modification.

Accordingly, claim 1 is believed to patentably define over the cited references.

Withdrawal of the rejections and allowance of claims 1-6 is respectfully requested.

Respectfully submitted,



Michael J. Ure, Reg. 33,089

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